

002020" FEET 360

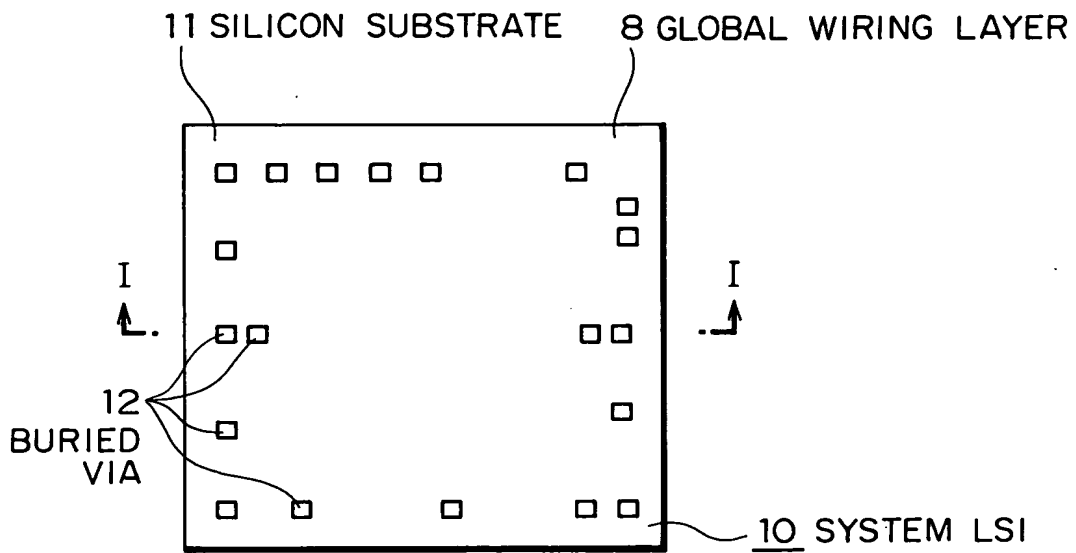


FIG. 1A

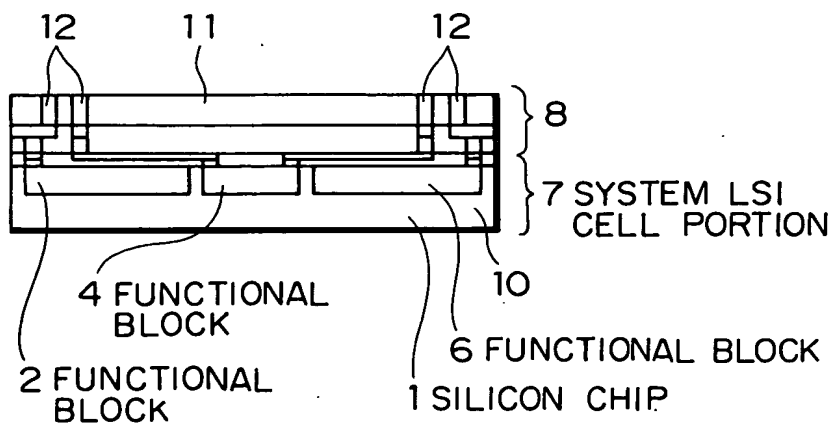
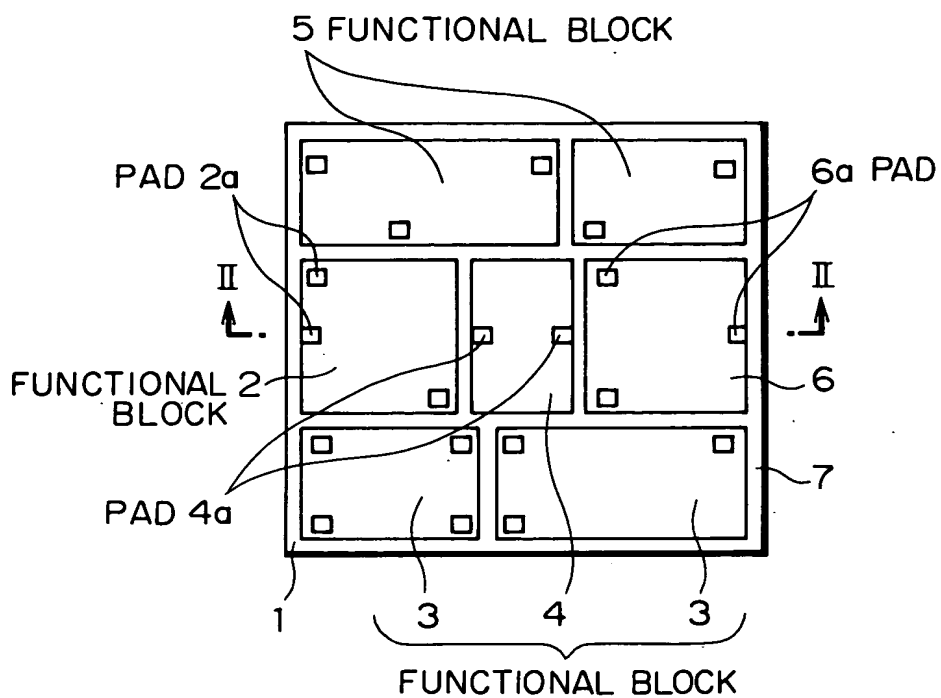


FIG. 1B

51795



00613331-070700

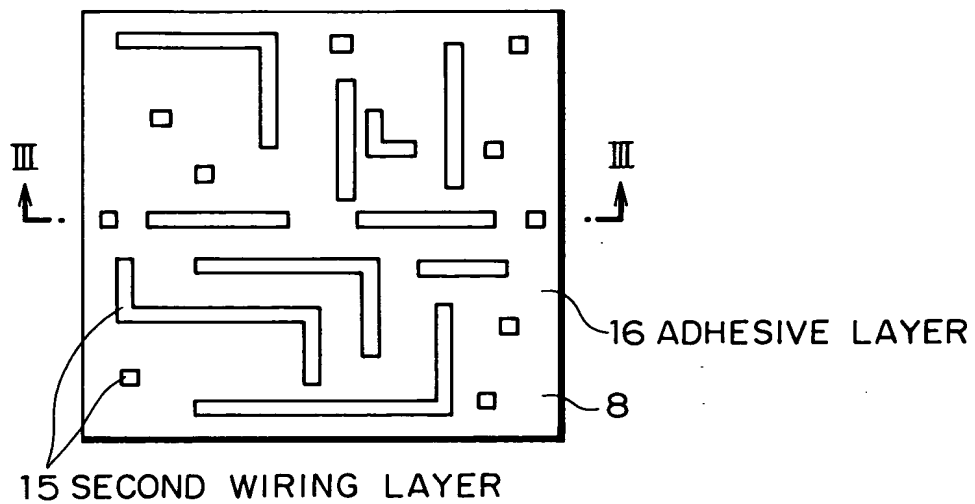


FIG. 3A

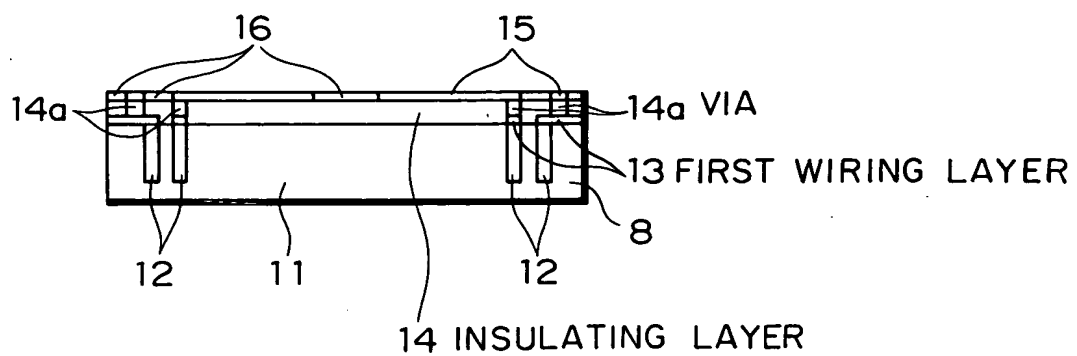


FIG. 3B



FIG. 4A

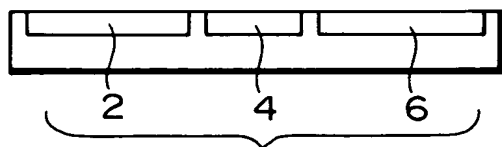


FIG. 4B

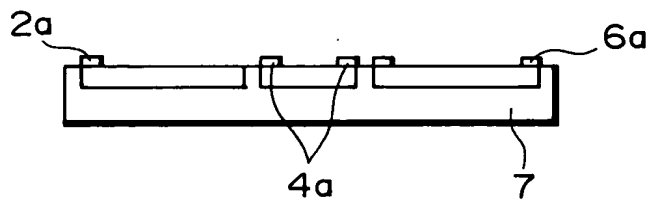


FIG. 4C



FIG. 5A

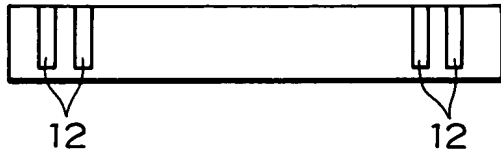


FIG. 5B

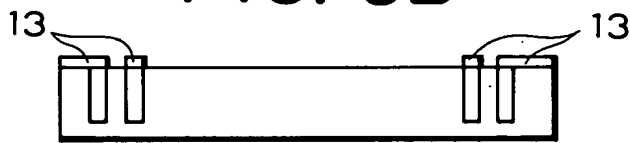


FIG. 5C

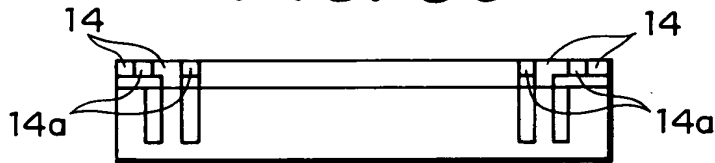


FIG. 5D

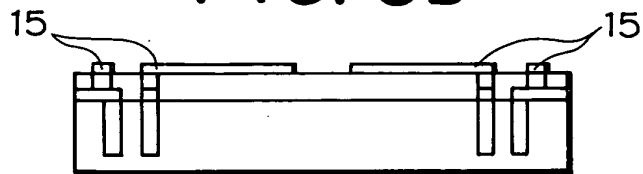


FIG. 5E

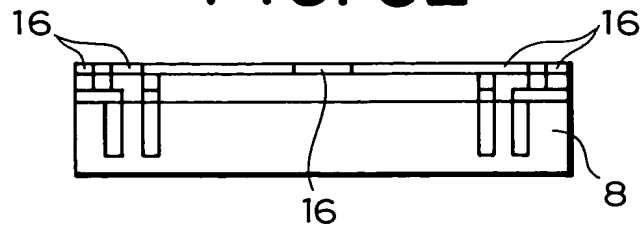


FIG. 5F

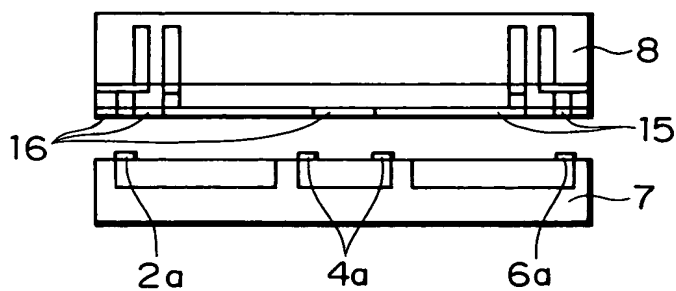


FIG. 6A

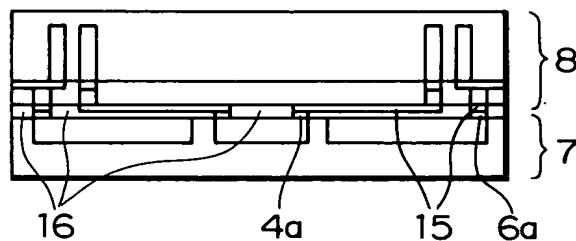


FIG. 6B

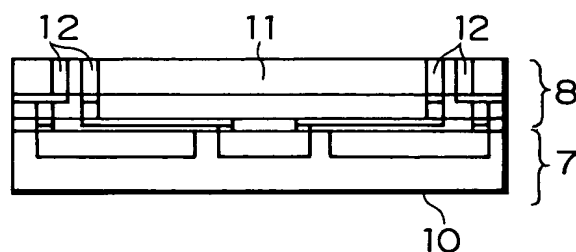


FIG. 6C

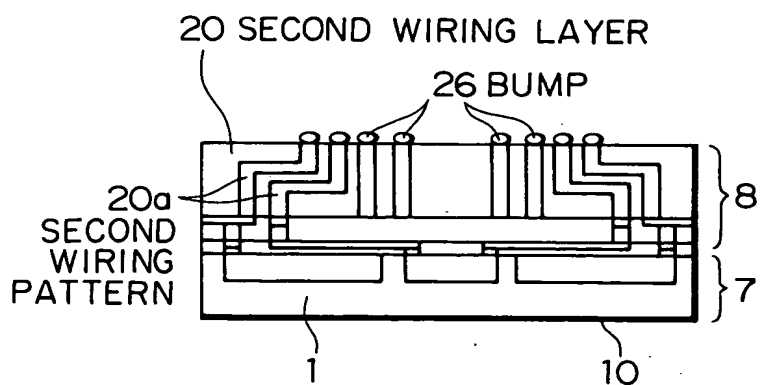


FIG. 7

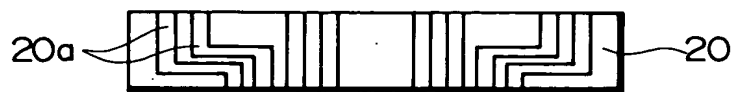


FIG. 8A



FIG. 8B

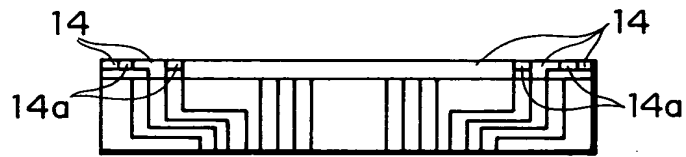


FIG. 8C

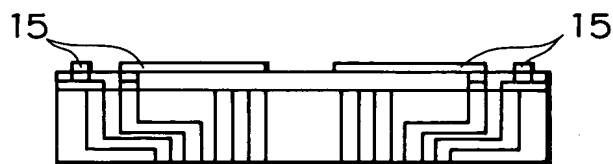


FIG. 8D

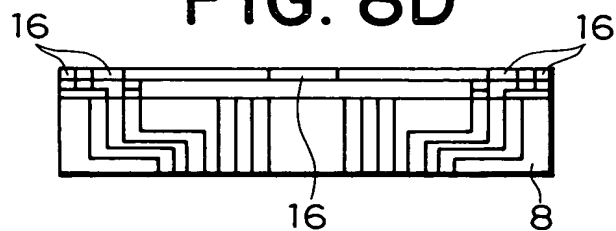


FIG. 8E

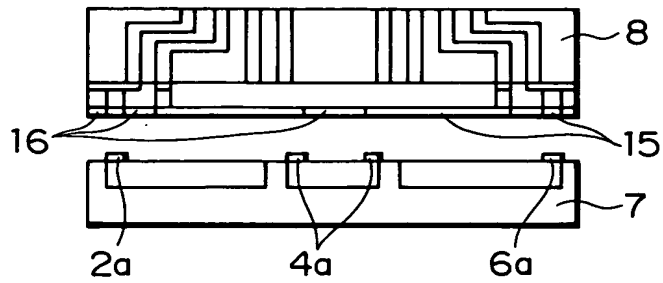


FIG. 9A

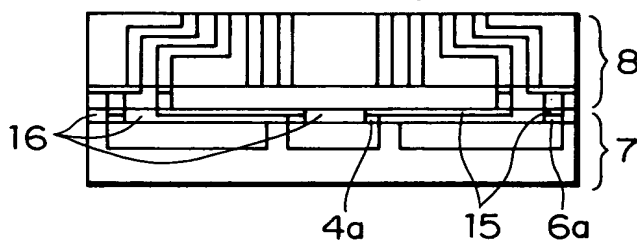


FIG. 9B

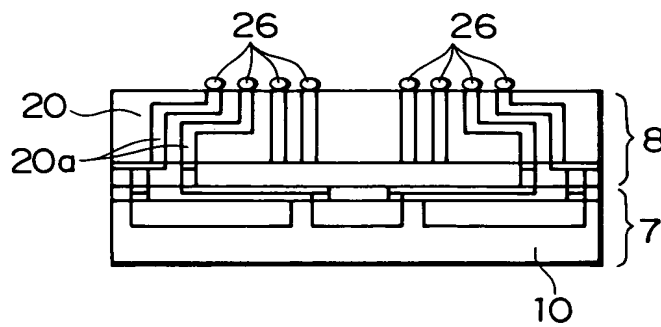


FIG. 9C



002020" TEEET960

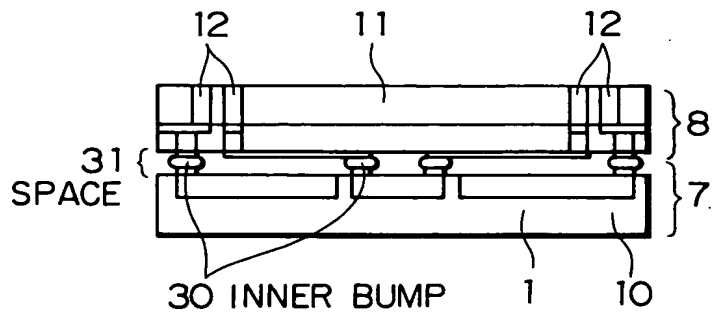


FIG. 10



FIG. 1 IA

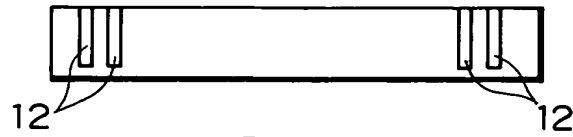


FIG. 1 IB

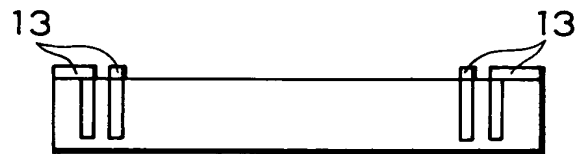


FIG. 1 IC

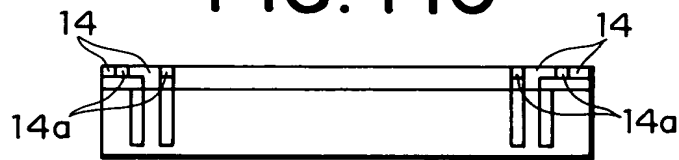


FIG. 1 ID

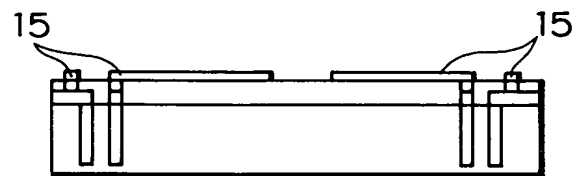


FIG. 1 IE

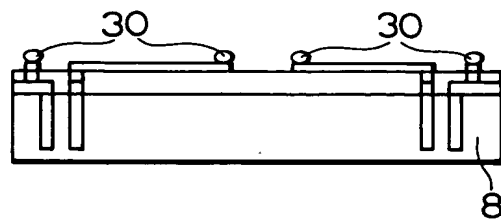
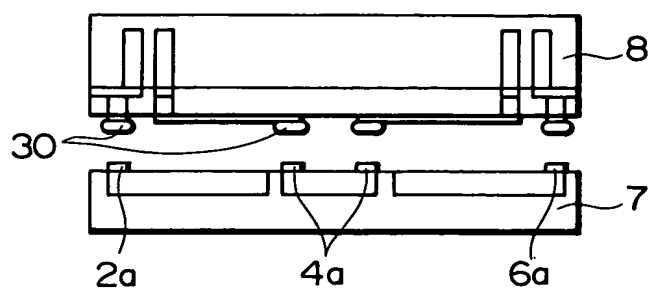
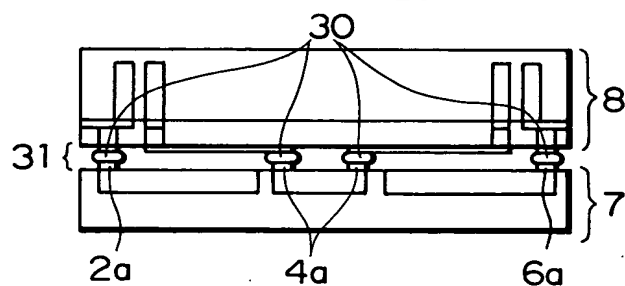


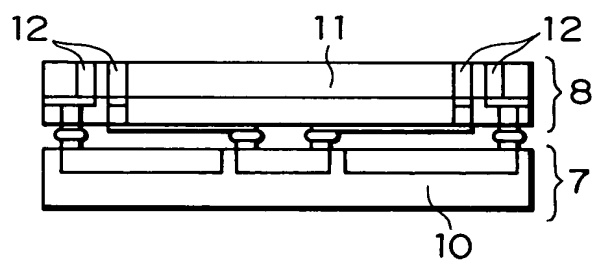
FIG. 1 IF



**FIG. 12A**



**FIG. 12B**



**FIG. 12C**

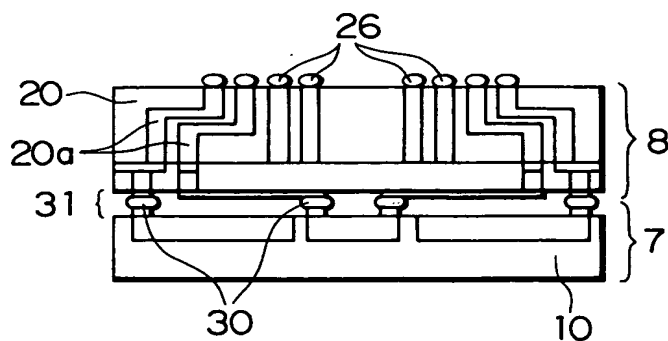


FIG. 13

A cross-sectional view of a substrate 20. A conductive pattern 20a is formed on the top surface of the substrate. The pattern consists of a central rectangular region and two sets of parallel lines extending outwards from the central region.

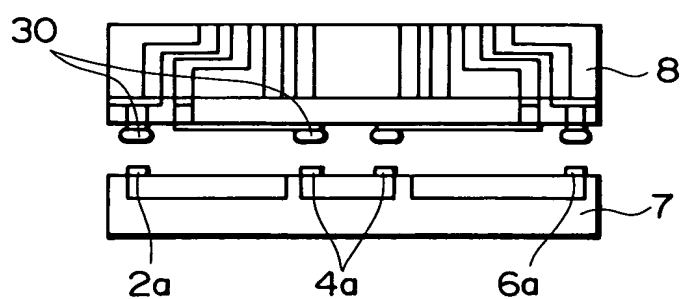
FIG. 14A

13 ← writing layer

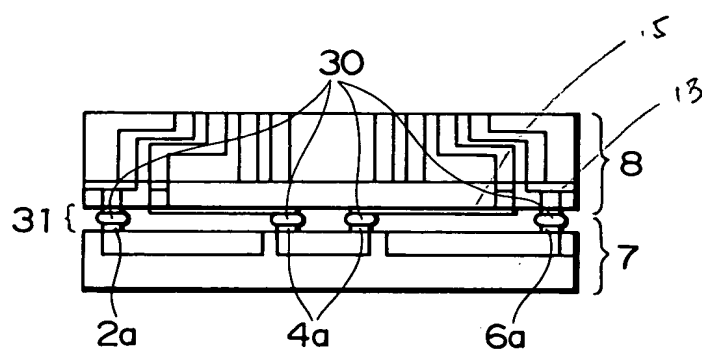
A cross-sectional view of a semiconductor device. It features a central channel region (14) and side regions (14a). The side regions (14a) are labeled with the handwritten note "insulating layer".

A diagram showing a 15-bit bus structure. It consists of a horizontal bar with 15 vertical lines extending downwards. A callout bubble points to the 15th line from the left, labeled "15".

A cross-sectional view of a semiconductor device. It shows a substrate labeled 8 with a series of vertical lines representing conductive regions. Two gate electrodes, each labeled 30, are positioned on top of the substrate, connected to the conductive regions below. The device is shown in a perspective view, with the gate electrodes extending along the length of the substrate.



**FIG. 15A**



**FIG. 15B**

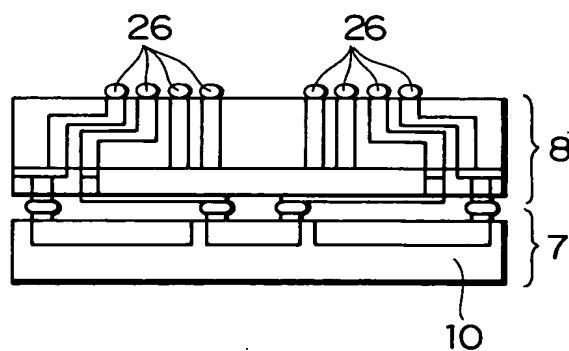


FIG. 15C

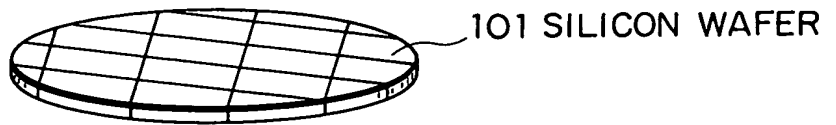


FIG. 16A



FIG. 16B



FIG. 16C

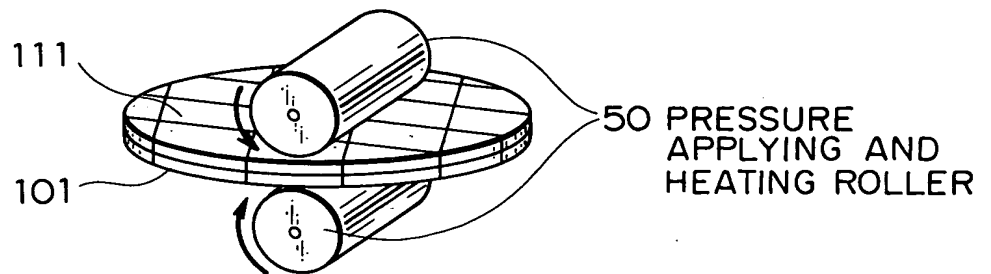


FIG. 16D

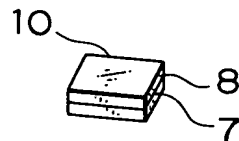


FIG. 16E